**v7.50.0.0**

***(Sept 30th, 2022)***

**IDesignSpec™ (IDS)**

**General Enhancements**

1. F#20369 - Support of memory width other than power of 2 or multiple of bus-width. [More Details](https://www.agnisys.com/release/docs/ids/Memory.html#memory_non_multiple)

**Bug Fixes**

**General**

1. F#20757 - Fixed error messaging in case of debug error in field entities.
2. F#20986 - Fix for repeating a section inside another section with "sv\_interface=true" property.
3. F#21341 - Fixed header indexing issue of AXI flopped widget (axi\_widget\_ff.v).
4. F#21425 - Fixed the issue of null pointer error when <block\_name>\_%d is used with -if switch in htmlalt2 output.
5. F#20681 - Fixed issue with "-tool VCS" switch when used in the command line in IDSWord configuration along with the property {widget=apb::apb\_widget}.
6. F#21231/F#20681 - Fixed issue regarding IDSWord-adv-plain license unencrypted widget file in IDS-Word.
7. F#20369 - Fixed issue of parity in case of ALM license in IDS-Word.
8. F#21425 - Fixed issue of null pointer exception error in HTMLalt2 output generation.
9. F#20435 - Fixed check generate issue in multiple back annotation in IDS-Word.
10. F#20369 - Fixed issue of reg width calculation of memory template with repeat in IDS-Word.
11. F#20965 - Fixed back annotation index calculation issue in IDS-Word.

**RTL**

1. F#21314 - Fixed buffer delay in clock assignment when using VHDL widget with an IDS generated Verilog RTL.
2. F#21288 - Fixed pprot connection issue with “reg\_clk” property in CDC.
3. F#21254 - Fix for “-dir\_out\_specific” switch with VHDL output.
4. F#21319 - Fixed reserved field issue in CRC.
5. F#21164 - Fixed reserved field issue in parity when used with “ecc\_sniffer” property.

**UVM**

1. F#21386 - Fixed create and configure declaration issues in case of subblock having an external section.